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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,177	07/08/2003	Bin Yu	H1130	7091
45114	7590	09/06/2005	EXAMINER	
HARRITY & SNYDER, LLP 11240 WAPLES MILL ROAD SUITE 300 FAIRFAX, VA 22030			ROSE, KIESHA L	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/614,177

Applicant(s)

YU ET AL.

Examiner

Kiesha L. Rose

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 14 and 17-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9, 14 and 17-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the RCE filed 20 July 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5,7-8,14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acovic et al. (U.S. Patent 5,411,905) in view of Fried et al. (U.S. Publication 2003/0178670).

Acovic discloses an EEPROM (Figs. 2 and 3) which contain a substrate, an insulating layer (10) formed on substrate that comprises a buried oxide layer, a silicon (conductive) fin structure (12) formed on the insulating layer and having a first and second side surface, a first polysilicon spacer (22) formed adjacent to the first side surface and acting as a first floating gate, a second polysilicon spacer (22) formed adjacent to the second side surface and acting as a second floating gate, a gate dielectric layer (24) formed on the first and second spacer and the top of the fin structure and acts as an inter-gate dielectric, a first gate (26) formed on the right side of the fin) formed on the insulating layer and disposed on the first side of the fin and a second gate (26) formed on the left side of the fin) formed on the second side of the fin

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and electrically isolated from each other and are programmed independently of each other, an oxide layer (20) formed on the first and second side surfaces of the fin and acting as a tunnel oxide layer with a width of 70 Angstroms, source and drain regions (Figs. 3 and 4) formed on insulating layer and disposed adjacent to the first and second side of the fin structure and a nitride/oxide dielectric cap (14/16) formed over a top surface of the fin structure. Acovic discloses all the limitations except for the gate dielectric layer and the first and second gate to contact the insulating layer. Whereas Fried discloses Finfet (Fig. 8) that comprises a substrate (90), an insulating layer (99) with a fin (100), a first and second spacer (115), a gate dielectric layer (116) that contacts the insulating layer and a control gate (120) that contacts the insulating layer. Even though it does not disclose the control gate as a first and second gate it can be seen in Acovic that the control gate and be separated and electrically isolated from each other. The gate dielectric layer and the control gate contact the insulating layer for after etching to make the device electrically isolated from the surrounding structures. (Paragraphs 36-38) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Acovic by having the gate dielectric layer and control gate to contact the insulating layer for electrical isolation from other surrounding structures as taught by Fried.

Claims 6,9 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acovic and Fried.

Acovic and Fried disclose all the limitations except for the width ranges of the first and second spacers and fin. It would have been obvious to one having ordinary skill

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in the art at the time the invention was made to have the first and second spacers width to be 100-500A and the width of the fin structure to be 100-1000A, since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. (1955)

Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acovic and Fried.

Acovic discloses an EEPROM (Figs. 2 and 3) which contain a substrate, an insulating layer (10) formed on substrate that comprises a buried oxide layer, a silicon fin structure (12) formed on the insulating layer and having a first and second side surface, a first polysilicon spacer (22) formed adjacent to the first side surface and acting as a first floating gate, a second polysilicon spacer (22) formed adjacent to the second side surface and acting as a second floating gate, a gate dielectric layer (24) formed on the first and second spacer and the top of the fin structure, a first gate (26 formed on the right side of the fin) formed on the insulating layer and disposed on the first side of the fin and a second gate (26 formed on the left side of the fin) formed on the second side of the fin and electrically isolated from each other and are programmed independently of each other, an oxide layer (20) formed on the first and second side surfaces of the fin and acting as a tunnel oxide layer with a width of 70 Angstroms, source and drain regions (Fig. 3) formed on insulating layer and disposed adjacent to the first and second side of the fin structure and a nitride/oxide dielectric cap (14/16) formed over a top surface of the fin structure. Acovic discloses all the limitations except

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for the width ranges of the first and second spacers and fin. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the width of the oxide layer to be 10-100A, the first and second spacers width to be 100A-500A and the gate dielectric to have a thickness of 50A-200A, since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. (1955) Acovic discloses all the limitations except for the first and second gate to contact the insulating layer. Whereas Fried discloses Finfet (Fig. 8) that comprises a substrate (90), an insulating layer (99) with a fin (100), a first and second spacer (115), a gate dielectric layer (116) and a control gate (120) that contacts the insulating layer. Even though it does not disclose the control gate as a first and second gate it can be seen in Acovic that the control gate and be separated and electrically isolated from each other. The control gate contacts the insulating layer for after etching to make the device electrically isolated from the surrounding structures. (Paragraphs 36-38) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Acovic by having the control gate to contact the insulating layer for electrical isolation from other surrounding structures as taught by Fried.

Response to Arguments

Applicant's arguments with respect to claims 1-9,14 and 17-22 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KP
KLR


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800